**ECE 3457**

**Lab 4: nMOS and CMOS Logic Gates**

Ethan Hitchcock (1408202)

**Goal:**

Study nMOS and CMOS logic gates.

Design, simulate (i.e. run MultiSim or PSPICE) and measure the response of the following logic gates. Use VDD = 5[V]. Construct a logic table for each gate by applying combinations of 0 and 5[V] inputs and measure the output voltages.

**Task A:**

2-input nMOS NOR and NAND gate with enhancement load.

**Task B:**

2-input CMOS NOR and NAND gate.

**Task C:**

2-input Pseudo-nMOS NOR and NAND gate.

**Theory:**

From Lab 1: (Task A, used to find simulation characteristics for transistors)

The CD4007 enhancement nMOS and pMOS transistors have gate, drain, and source pins. The transistor has the equations

for when the transistor is operating in the triode region (VGS > VT and VDS ≤ VGS – VT) and

for when the transistor is operating in the saturation region (VGS > VT and VDS > VGS – VT). As the transistor enters the saturation region, the ID curve will begin to plateau. This is because the equation for current through the drain and source pins is not dependent on VDS when the transistor is operating in the saturation region. By obtaining the nMOS and pMOS transistors’ iv curves for different VGS values, it becomes possible to derive the value of K where

We can calculate the value of K and VT by plotting the square root of IDS against VGS according to the linear equation

Where the square root of K is the slope and VT is the x-intercept.

Lab 4: (Task B & C)

A transistor has 3 states: cutoff region, triode region, and saturation region. The transistor acts as an open circuit in the cutoff region, as such no current will flow. In the triode region, the current varies so the voltage across the transistor will also vary. When the transistor is operating in saturation mode, it’s current should no longer be changing dramatically so it acts like a small resistor, resulting in a small voltage reading across the transistor. As the transistor acts like an open circuit in the cut off region, it can be used like a logic switch by varying the gate voltage. Using variations of nMOS configurations in the Pull-Down Network, it is possible to achieve different logic functions. Different load circuits will result in different high output voltages and low output voltages.

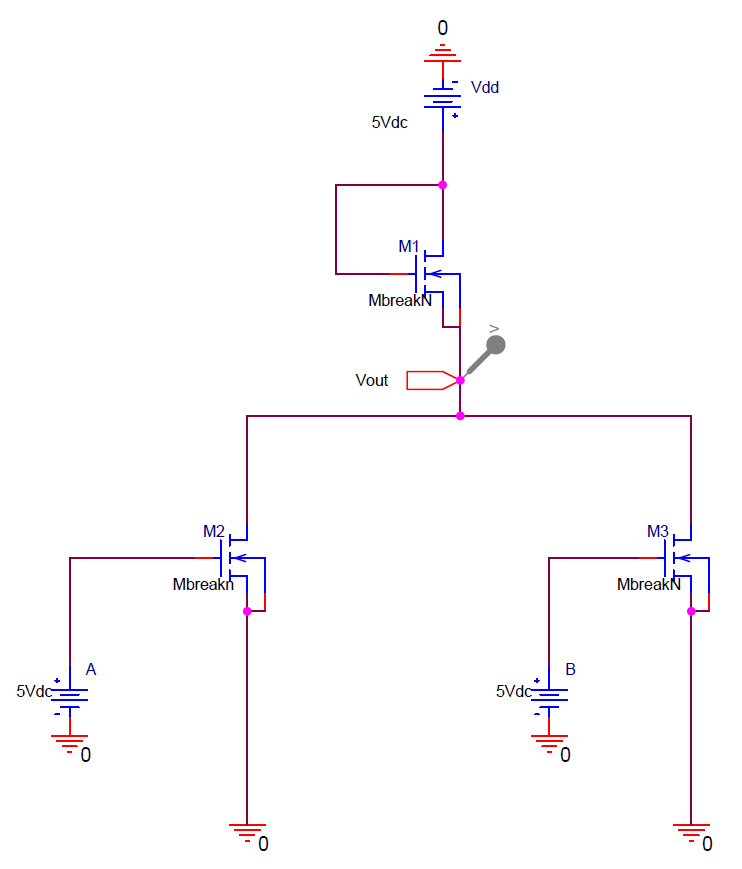
**Simulation & Experiment:**

For all tasks following, simulation values were found in Lab 1. The values for the nMOS are Kn is 685.6[μA/V2], and VT is 0.91[V]. The values for the pMOS are Kp is 635.2[μA/V2], and VT is 1.32 [V].

**Task A:**

**2-input nMOS NOR Gate with Enhancement Load:**

The circuit was designed such that there would be two inputs, A and B, which would be used to simulate a logic function and the output would be measured at Vout. The below circuit realizes the logic equation Vout = ͞A·͞B commonly known as a NOR gate.

 *Figure 1: 2-input nMOS NOR Gate with Enhancement Load*

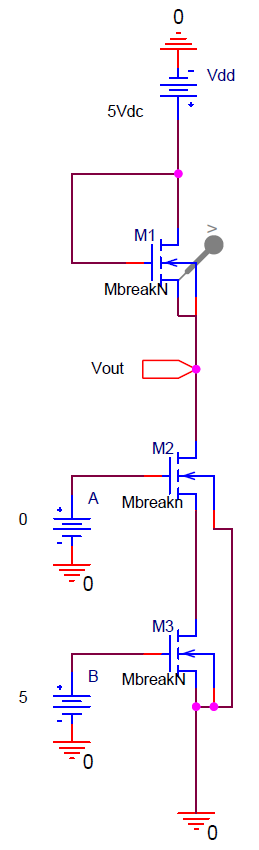
The load nMOS acts as an enhancement load as its gate is connected to the 5[V] source voltage, thus only operating in its saturation mode. The inputs to gates A and B are varied between 0[V] representing logic 0 and 5[V] representing logic 1. The following data was retrieved from simulations and experiments.

*Table 1: Output for 2-input nMOS NOR Gate with Enhancement Load*

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | Vout Simulated [V] | Vout Experiment [V] |
| 0 | 0 | 4.0899 | 4.021 |
| 0 | 1 | 1.1979 | 1.210 |
| 1 | 0 | 1.1979 | 1.223 |
| 1 | 1 | 0.7505 | 0.512 |

**2-input nMOS NAND Gate with Enhancement Load:**

The circuit was designed such that there would be two inputs, A and B, which would be used to simulate a logic function and the output would be measured at Vout. The below circuit realizes the logic equation Vout = ͞A+͞B commonly known as a NAND gate.

*Figure 2: 2-input nMOS NAND Gate with Enhancement Load*

The following data was retrieved from simulations and experiments.

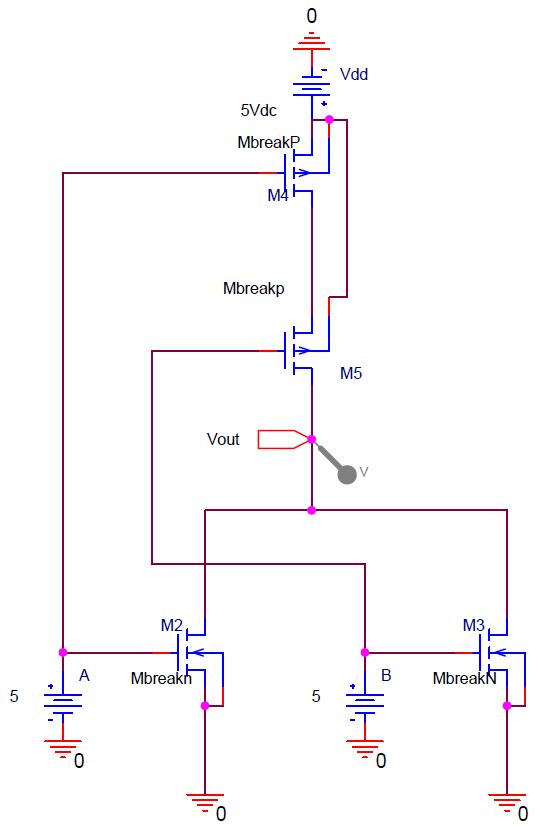
*Table 2: Output for 2-input nMOS NAND Gate with Enhancement Load*

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | Vout Simulated [V] | Vout Experiment [V] |
| 0 | 0 | 4.0899 | 4.051 |
| 0 | 1 | 4.0899 | 4.051 |
| 1 | 0 | 4.0898 | 4.050 |
| 1 | 1 | 1.7286 | 0.998 |

**Task B:**

**2-input CMOS NOR Gate:**

The circuit was designed such that there would be two inputs, A and B, which would be used to simulate a logic function and the output would be measured at Vout. The below circuit realizes the logic equation Vout = ͞A·͞B commonly known as a NOR gate.

*Figure 3: 2-input CMOS NOR Gate*

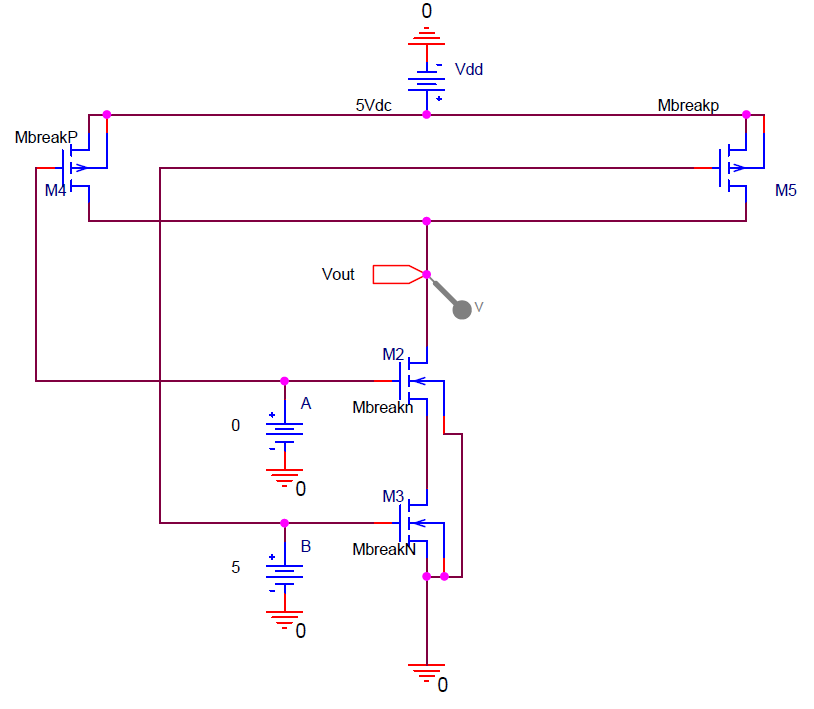
The pull-up network is connected to the 5[V] source voltage and the pull-down network is connected to ground. This circuit should realize output voltages of 0[V] and 5[V]. The inputs to gates A and B are varied between 0[V] representing logic 0 and 5[V] representing logic 1. When logic for a gate is high, the corresponding pMOS is turned off, while the corresponding nMOS is turned on. The following data was retrieved from simulations and experiments.

*Table 3: Output for 2-input CMOS NOR Gate*

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | Vout Simulated [V] | Vout Experiment [V] |
| 0 | 0 | 5.000 | 5.030 |
| 0 | 1 | 1.787[nV] | 0.007 |
| 1 | 0 | 4.418[nV] | 0.001 |
| 1 | 1 | 0.893[nV] | 0.004 |

**2-input CMOS NAND Gate:**

The circuit was designed such that there would be two inputs, A and B, which would be used to simulate a logic function and the output would be measured at Vout. The below circuit realizes the logic equation Vout = ͞A+͞B commonly known as a NAND gate.



*Figure 4: 2-input CMOS NAND Gate*

The following data was retrieved from simulations and experiments.

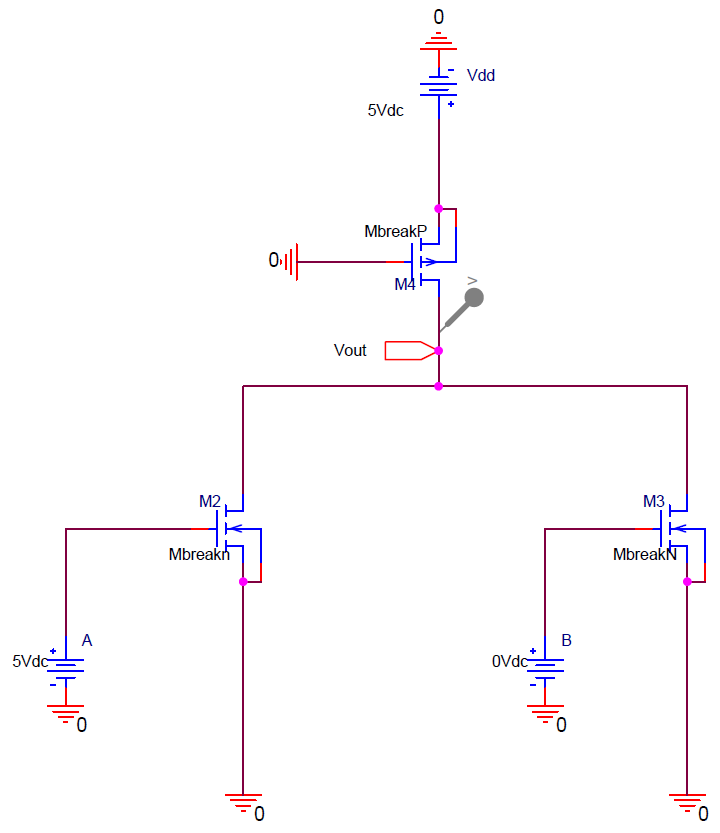
*Table 4: Output for 2-input CMOS NAND Gate*

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | Vout Simulated [V] | Vout Experiment [V] |
| 0 | 0 | 5.000 | 5.037 |
| 0 | 1 | 5.000 | 5.037 |
| 1 | 0 | 5.000 | 5.037 |
| 1 | 1 | 7.147[nV] | 0.004 |

**Task C:**

**2-input Pseudo-nMOS NOR Gate:**

The circuit was designed such that there would be two inputs, A and B, which would be used to simulate a logic function and the output would be measured at Vout. The below circuit realizes the logic equation Vout = ͞A·͞B commonly known as a NOR gate.

*Figure 5: 2-input Pseudo-nMOS NOR Gate*

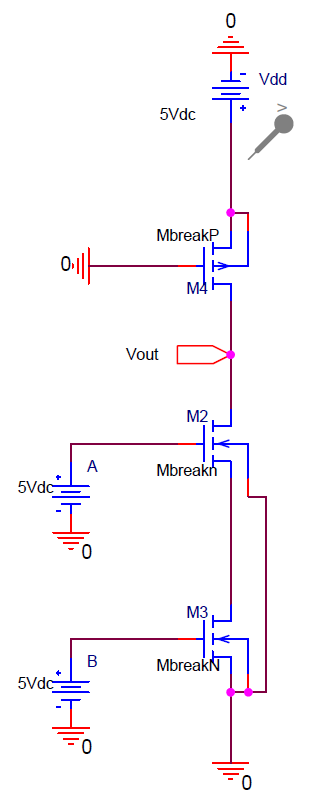
The load pMOS gate is connected to ground, thus acting as a pseudo-nMOS transistor. The inputs to gates A and B are varied between 0[V] representing logic 0 and 5[V] representing logic 1. The following data was retrieved from simulations and experiments.

*Table 5: Output for 2-input Pseudo-nMOS NOR Gate*

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | Vout Simulated [V] | Vout Experiment [V] |
| 0 | 0 | 5.0000 | 5.033 |
| 0 | 1 | 1.9546 | 0.998 |
| 1 | 0 | 1.9556 | 1.414 |
| 1 | 1 | 0.8566 | 0.505 |

**2-input Pseudo-nMOS NAND Gate:**

The circuit was designed such that there would be two inputs, A and B, which would be used to simulate a logic function and the output would be measured at Vout. The below circuit realizes the logic equation Vout = ͞A+͞B commonly known as a NAND gate.

  
*Figure 6: 2-input Pseudo-nMOS NAND Gate*

The following data was retrieved from simulations and experiments.

*Table 6: Output for 2-input Pseudo-nMOS NAND Gate*

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | Vout Simulated [V] | Vout Experiment [V] |
| 0 | 0 | 5 | 5.044 |
| 0 | 1 | 5 | 5.044 |
| 1 | 0 | 5 | 5.045 |
| 1 | 1 | 3.490 | 3.408 |

**Analysis:**

As expected, the load circuit determined the logic high output voltage and logic low output voltage and all circuits achieved their respective logic functions. For Task A: NOR Gate, by simulation, the high output voltage was 4.0899[V] which would register as logic 1, and the low output voltage was 1.1979[V] which would register as logic 0. The experimental results met the simulated expectations. For Task A: NAND Gate, by simulation, the high output voltage was 4.0899[V] which would register as logic 1, and the low output voltage was 1.7286[V] which would register as logic 0. The experimental results were generally within expectations, however, there was a 1[V] difference in simulated value and experimental value for the case where A = 1, and B = 1. For Task B: NOR Gate, by simulation, the high output voltage was 5 [V] which would register as logic 1, and the low output voltage was ~0[V] which would register as logic 0. The experimental data matched expectations. For Task B: NAND Gate, by simulation, the high output voltage was 5[V] which would register as logic 1, and the low output voltage was ~0[V] which would register as logic 0. The experimental data met expectations. For Task C: NOR Gate, by simulation, the high output voltage was 5[V] which would register as logic 1, and the low output voltage was 1.9556[V] which would register as logic 0. Generally, experimental data met expectations, but for the case when A = 0, and B = 1, the voltage was lower than anticipated. This may be due to differences in the characteristics of each transistor on the chip. This would cause discrepancies between simulation and experimental data as simulated data assumes all the transistors have the same characteristics. Alternately, this could be due to ongoing issues with getting the pMOS to operate to expectations throughout the semester due to unintentional misuse of the chip. Lastly, for Task C: NAND Gate, by simulation, the high output voltage was 5[V] which would register as logic 1, and the low output voltage was 3.490[V] which would register as logic 0. Experimental data met expectations. It can also be seen that for all the NOR gate circuits, the output voltage for the state where both A = 1, and B = 1, is lower than the states where one of A and B is at logic 1 and the other is at logic 0.

**Experimental Data:**

Logic 0 = 0[V]

Logic 1 = 5[V]

**Simulation Results:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Step A: Nor | |  |  | Step A: Nand | |  |
| A | B | Vout [V] |  | A | B | Vout [V] |
| 0 | 0 | 4.0899 |  | 0 | 0 | 4.0899 |
| 0 | 1 | 1.1979 |  | 0 | 1 | 4.0899 |
| 1 | 0 | 1.1979 |  | 1 | 0 | 4.0898 |
| 1 | 1 | 0.7505 |  | 1 | 1 | 1.7286 |
|  |  |  |  |  |  |  |
| Step B: Nor | |  |  | Step B: Nand | |  |
| A | B | Vout [V] |  | A | B | Vout [V] |
| 0 | 0 | 5 |  | 0 | 0 | 5 |
| 0 | 1 | 1.787[nV] |  | 0 | 1 | 5 |
| 1 | 0 | 4.418[nV] |  | 1 | 0 | 5 |
| 1 | 1 | 0.893[nV] |  | 1 | 1 | 7.147[nV] |
|  |  |  |  |  |  |  |
| Step C: Nor | |  |  | Step C: Nand | |  |
| A | B | Vout [V] |  | A | B | Vout [V] |
| 0 | 0 | 5 |  | 0 | 0 | 5 |
| 0 | 1 | 1.9546 |  | 0 | 1 | 5 |
| 1 | 0 | 1.9556 |  | 1 | 0 | 5 |
| 1 | 1 | 0.8566 |  | 1 | 1 | 3.49 |

**Experimental Results:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Step A: Nor | |  |  | Step A: Nand | |  |
| A | B | Vout [V] |  | A | B | Vout [V] |
| 0 | 0 | 4.021 |  | 0 | 0 | 4.051 |
| 0 | 1 | 1.21 |  | 0 | 1 | 4.051 |
| 1 | 0 | 1.223 |  | 1 | 0 | 4.05 |
| 1 | 1 | 0.512 |  | 1 | 1 | 0.998 |
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|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
| Step B: Nor | |  |  | Step B: Nand | |  |
| A | B | Vout [V] |  | A | B | Vout [V] |
| 0 | 0 | 5.03 |  | 0 | 0 | 5.037 |
| 0 | 1 | 0.007 |  | 0 | 1 | 5.037 |
| 1 | 0 | 0.001 |  | 1 | 0 | 5.037 |
| 1 | 1 | 0.004 |  | 1 | 1 | 0.004 |
|  |  |  |  |  |  |  |
| Step C: Nor | |  |  | Step C: Nand | |  |
| A | B | Vout [V] |  | A | B | Vout [V] |
| 0 | 0 | 5.033 |  | 0 | 0 | 5.044 |
| 0 | 1 | 0.998 |  | 0 | 1 | 5.044 |
| 1 | 0 | 1.414 |  | 1 | 0 | 5.045 |
| 1 | 1 | 0.505 |  | 1 | 1 | 3.408 |